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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/994,009 | 11/05/2001 | Fereidoon Heydari | 01-S-023 (1678-39) | 8816 |
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30431 7590 10/26/2006

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| EXAMINER |
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RODRIGUEZ, GLENDA P

| ART UNIT | PAPER NUMBER |
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2627

DATE MAILED: 10/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 09/994,009 | HEYDARI ET AL. | |
| | Examiner | Art Unit | |
| | Glenda P. Rodriguez | 2627 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 August 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 and 32-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30, 32-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-30, 32-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Patapoutian et al. (US Patent No. 5, 661, 760).

Regarding Claim 1, Patapoutian et al. teaches a coded binary sequence, comprising:

A first group of consecutive bits, the first group having first and second separate portions and representing one of a logic 1 and a logic 0, the bits in the first portion each having a first state and the bits in the second portion having a second state (See Col. 7, L. 29-30, wherein logic 1 has the state "--++" and logic 0 has the state "++--". It is inherent that a group of bits such as "10" will be encoded into "--++++--", making then two bits, each with its own independent state.); and

A second group of consecutive bits separate from the first group and each having a same state, the second group representing only the other of the logic 1 and the logic 0 (It is inherent to a person of ordinary skill in the art that if a second separate group of bits, all being the same state, such as "11" or "00", they will have the same state once these bits are coded. Hence, "11" will be encoded as "--++--++" and "00" will be "++--++--", both having the same state in each case.).

Claims (4 and 8) have limitations similar to those treated in the above rejection, and are met by the references as discussed above.

Claim 10 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 10 however also recites the following limitations: "disk sectors operable to store application data and servo wedges that store servo data" (Pat. No. 5, 661, 760; Col. 6, Lines 15-61 and Col. 6, Lines 15-61).

Claim 11 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 11 however also recites the following limitations: "a Viterbi detector" (Pat. No. 5, 661, 760; See Abstract).

Claim 14 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 14 however also recites the following limitations: "a sample circuit (Col. 3, L. 31-32) operable to generate samples of a signal that represents a coded binary sequence having a first group of consecutive bits each having a first logic level and a second group of consecutive bits (It is inherent that bits can be encoded as grouped bits, See also Col. 5, L. 64 to Col. 6, L. 4, wherein it samples at every period T, hence making groups of bits of T duration.), the second group having first and second portions, the bits in the first portion having the first logic level and the bits in the second portion having a second logic level (Hence, if "11" was sampled, this would be encoded as one logic level due to the fact that it is the same logic number), the first group representing only the first logic level and the second group representing the second logic level (Hence, if the first group having the same logic level "11" and the second logic level could be "00" and therefore is the second logic level compared to the

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“11” as given earlier. Thus, the first group, say “11” represents only a first logic level and the second, say “00” or “10” or “01” could be the second logic level.)”.

Claim 16 has limitations similar to those treated in the above rejection(s), and are met by the references as discussed above. Claim 14 however also recites the following limitations: “a data storage disk having a surface, data sectors at respective locations of the surface, and servo wedges that store servo data, a motor, a read head and a read head positioning circuit and a servo circuit” (Pat. No. 5, 661, 760; Col. 5, Lines 15-21 and Col. 6, Lines 15-61, Servo data are used for non-application purposes).

Method claim (20) is drawn to the method of using the corresponding apparatus claimed in claims (1, 4, 8, 10, 11, 14, and 16). Method Claim 20 also recites: “coding one of a logic 1 and a logic 0 as a first group of consecutive bits, the first group having a first and second equally sized portions (Col. 3, Lines 55-58. Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary 1s into “--++” and binary zeros into “++--”, each having two differing states. It is inherent that if a sequence of for example “1011” (“10” being a first logic level and “11” being a second logic level) will be encoded into “--++++----++--++”, having a first and second equally sized portion in the first group (“--++” and “++--”) having a second logic level (“1”) and a third logic level (“0”) (The description of Patent Application is according to the instant specification, and, it is concurrent with Page 6, Table 1 to Page 7, Line 13 of the instant specification.).)”

Method claims (24 and 27) are drawn to the method of using the corresponding apparatus claimed in claims (1, 4, 8, 10, 11, 14, and 16). Therefore method claims (24 and 27) correspond to apparatus claims (1, 4, 8, 10, 11, 14, and 16) and are rejected for the same reasons of anticipation as used above.

Claims (32 and 33) have limitations similar to those treated in the above rejections, and are met by the references as discussed above.

Regarding Claim 2, Patapoutian et al. teach all the limitations of Claim 1. Patapoutian et al. further teach wherein the first and second portions of the first group respectively comprise first and second halves of the first group (Pat. No. 5, 661, 760; Col. 3, Lines 55-58. Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that the first group with two portions (group "10") can be divided in to first and second halves: "10" or "--++++--" can be divided into "--++" and "++--".).

Regarding Claim 6, Patapoutian et al. teach all the limitations of Claim 1. Patapoutian et al. further teach wherein the first and second groups each respectively comprise four consecutive bits (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary ones into "--++" and binary zeros into "++--").).

Regarding Claim 7, Patapoutian et al. and teach all the limitations of Claim 4. Patapoutian et al. further teach the first and second portions of the second group respectively comprises first and second halves of the second group ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1").).

Regarding Claim 12, Patapoutian et al. teach all the limitations of Claim 11. Patapoutian et al. further teaches wherein the binary sequence comprises a coded binary sequence (See Abstract).

Regarding Claim 13, Patapoutian et al. teach all the limitations of Claim 11. Patapoutian et al. further teach wherein the first logic level comprises a logic 0; and the second logic level comprises a logic 1 (Col. 3, Lines 55-58. Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that if a sequence of for example "10" will be encoded into "--++++--", having a first and second equally sized portion in the first group ("--++" and "++--").).

Regarding Claim 15, Patapoutian et al. teach all the limitations of Claim 14. Patapoutian et al. further teach a decoder coupled to the Viterbi detector and operable to decode the recovered binary sequence (Col. 11, Lines 3-25 and Lines 57-62).

Regarding Claim 17, Patapoutian et al. teach all the limitations of Claim 16. Patapoutian et al. further teaches wherein the servo circuit comprises: a sample circuit operable to generate samples of the servo signal (See Abstract); and a Viterbi detector coupled to the sample circuit and operable to recover the servo data from the samples of the servo signal (Col. 5, Line 64 to Col. 6, Line 13 and Abstract and Fig. 1).

Regarding Claim 18, Patapoutian et al. teach all the limitations of Claim 16. Patapoutian et al. further teaches wherein the servo circuit comprises a decoder operable to decode the recovered servo data (See Abstract. Patapoutian et al. teaches that the Viterbi detector also decodes the $\frac{1}{4}$ signal.).

Regarding Claim 19, Patapoutian et al. teach all the limitations of Claim 16. Patapoutian et al. further teach wherein the read head comprises a read-write head (Col. 5, Lines 15-21, Lines 28-32 and Lines 57-63 and Col. 12, Lines 1-12).

Regarding Claim 22, Patapoutian et al. teach all the limitations of Claim 20. Patapoutian et al. further teaches wherein the coding comprises: coding the one of the logic 1 and the logic 0 as a first group of four consecutive bits (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Col. 3, Lines 55-58. Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary ones into “--++” and binary zeros into “++--”); and coding the other of the logic 1 and the logic 0 as a second group of four consecutive bits (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary ones into “--++” and binary zeros into “++--”).).

Regarding Claim 23, Patapoutian et al. teach all the limitations of Claim 20. Patapoutian et al. further teach wherein the first and second portions of the first group respectively comprise first and second halves of the first group (“11” would be the second group (fourth logic level) which also has two equally sized portions (“--++” and “--++”) having a fourth logic level (“1”) and a fifth logic level (“1”).).

Regarding Claim 28, Patapoutian et al. teach all the limitations of Claim 27. Patapoutian et al. further teaches wherein: the first and second code symbols each comprise a number of code bits (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Col. 3, Lines 55-58). Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary ones into “--++” and binary zeros into “++--”); and the lengths of the first and second code symbols are each less than the product of the number and a length of a servo-bit region (Patapoutian et al. teaches that each group of bits consists of 4 consecutive bits (Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary ones into “--++” and binary zeros into “++--”).).

Regarding Claims 25, 26 and 29, Patapoutian et al. teach all the limitations of Claims 24 and 27, respectively. Patapoutian et al. further teach wherein: the first logical bit equals a logic 0; and the second logical bit equals a logic 1 (Col. 3, Lines 55-58. Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that these logic levels can be achieved according to the configuration of zeros and ones that the disk drive enhances.).

Regarding Claim 30, Patapoutian et al. teach all the limitations of Claim 27. Patapoutian et al. further teaches wherein each of the first and second groups of code words is or is approximately half as long as the first code word ("11" would be the second group (fourth logic level) which also has two equally sized portions ("--++" and "--++") having a fourth logic level ("1") and a fifth logic level ("1").).

Regarding Claims 3, 5, 9, 21 and 34, Patapoutian et al. teach all the limitations of Claims 1, 4, 8, 20 and 34, respectively. Patapoutian et al. further teach wherein the first and second groups respectively represent logic 1 and logic 0; the first and second states respectively equal logic 0 and logic 1; and the second group of consecutive bits each has a state of logic 0 (Col. 3, Lines 55-58. Patapoutian et al. teaches a $\frac{1}{4}$ coding scheme that codes binary ones into "--++" and binary zeros into "++--". It is inherent that these logic levels can be achieved according to the configuration of zeros and ones representing the data to be recorded.).

Response to Arguments

3. Applicant's arguments filed 08/07/06 have been fully considered but they are not persuasive. Even though the Claims have been amended, the Claims remain rejected under USC 102 (b) due to the reasons stated in the above rejection.

Conclusion

4. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

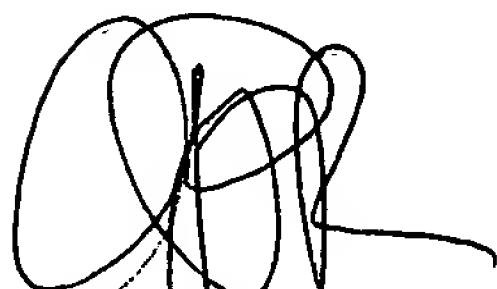
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (571) 272-7561. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

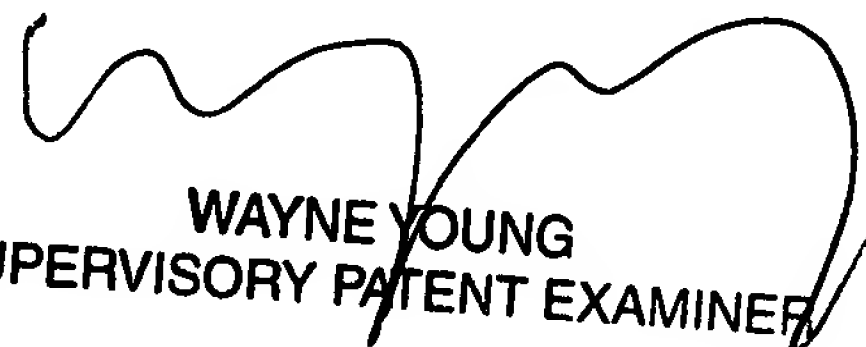
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on (571) 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



gpr
10/17/06.



WAYNE YOUNG
SUPERVISORY PATENT EXAMINER